Claims

1. A storage device, comprising:

a first semiconducting layer having a p-dopant, said first semiconducting layer;

a second semiconducting layer having an n-dopant, said second semiconducting layer disposed on said first semiconducting layer;

a junction formed between said first and said second semiconducting layers;

a charge trapping structure disposed on said second semiconducting layer; and

a conductive gate, wherein said conductive gate and said charge trapping structure move relative to the other, wherein an electric field applied across said second semiconducting layer and said conductive gate traps charge in said charge trapping structure.

2. The storage device in accordance with claim 1, further comprising a substrate, wherein said first semiconducting layer is disposed on or in said substrate.

3. The storage device in accordance with claim 2, wherein said substrate further comprises a p-doped substrate, wherein said first semiconducting layer is disposed in said p-doped substrate.

4. The storage device in accordance with claim 2, wherein said substrate further comprises a doped substrate having a dielectric layer disposed on said doped substrate, and wherein said first semiconducting layer further comprises an epitaxial p-doped semiconductor layer formed on said dielectric layer.

5. The storage device in accordance with claim 4, wherein said second semiconducting layer further comprises an epitaxial n-doped semiconductor layer formed on said epitaxial p-doped semiconductor layer.

6. The storage device in accordance with claim 2, wherein said substrate is either a semiconductor substrate or an inorganic substrate.

7. The storage device in accordance with claim 1, wherein said charge trapping structure further comprises:

a first dielectric layer disposed on said second semiconducting layer;

a second dielectric layer disposed on said first dielectric layer; and

a third dielectric layer disposed on said second dielectric layer.

8. The storage device in accordance with claim 7, wherein said first and third dielectric layers are formed from an inorganic dielectric material.

9. The storage device in accordance with claim 7, wherein said first and said second dielectric layers form a charge trapping interface, whereby charge is trapped at said charge trapping interface.

10. The storage device in accordance with claim 7, wherein said first and said third dielectric layers are formed from silicon oxide, and wherein said second dielectric layer is formed from silicon nitride.

11. The storage device in accordance with claim 1, wherein said charge trapping structure further comprises nano-particles dispersed within a dielectric medium.

12. The storage device in accordance with claim 11, wherein said nano-particles further comprise electrically conductive nano-particles.

13. The storage device in accordance with claim 11, wherein said nano particles further comprise germanium nano-particles.

14. The storage device in accordance with claim 1, further comprising:

a first electrical conductor electrically coupled to said first semiconducting layer; and

a second electrical conductor electrically coupled to said second semiconducting layer.

15. The storage device in accordance with claim 1, further comprising a micromover coupled either to said conductive gate or to said charge trapping structure, wherein said micromover moves either said conductive gate or said charge trapping structure in at least one lateral dimension.

16. The storage device in accordance with claim 15, wherein said micromover moves either said conductive gate or said charge trapping structure in at least one lateral dimension and said conductive gate is not in contact with said charge trapping structure.

17. The storage device in accordance with claim 15, wherein said micromover moves either said conductive gate or said charge trapping structure laterally in two dimensions.

18. The storage device in accordance with claim 15, wherein said micromover moves either said conductive gate or said charge trapping structure laterally in three dimensions.

19. The storage device in accordance with claim 15, wherein said micromover further comprises a tip actuator coupled to said conductive, wherein said tip actuator moves said conductive gate to control a distance between said conductive gate and said charge trapping storage structure.

20. The storage device in accordance with claim 19, wherein said tip actuator moves said conductive gate in three mutually perpendicular directions.

21. The storage device in accordance with claim 15, wherein said micromover further comprises:

a frame, wherein said micromover is configured to move relative to said frame; and

a mechanical suspension having a plurality of suspension subassemblies operatively coupled between said frame and said micromover, each suspension subassembly including:

at least one resilient mover flexure secured between said micromover and a coupling member, and

at least two resilient frame flexures secured between said coupling member and said frame, said frame flexures disposed on opposing sides of said mover flexure and aligned along a longitudinal axis passing through said mover flexure.

22. The storage device in accordance with claim 21, wherein said coupling member of each of said suspension subassemblies tracks relative movement of said micromover in a first direction while remaining substantially independent of relative movement in a second direction perpendicular to said first direction.

23. The storage device in accordance with claim 15, wherein said micromover further comprises:

a frame, wherein said micromover is configured to move relative to said frame, said micromover including a plurality of data locations accessible via operation of a read/write device; and

a mechanical suspension operatively coupled between said frame and said micromover, said mechanical suspension allowing planar movement of said micromover relative to said frame and substantially preventing out of plane relative movement, said planar movement defined by an X direction and a Y

direction, said mechanical suspension including:

at least one X-axis flexure flexing in response to movement of the micromover in said X-direction relative to said frame, and

at least on Y-axis flexure flexing in response to movement of the micromover in said Y-direction relative to said frame.

24. The storage device in accordance with claim 1, wherein said conductive gate further comprises:

a base structure having an outer surface; and

an outer layer disposed on said outer surface of said base structure.

25. The storage device in accordance with claim 24, wherein said base structure is formed utilizing a conductive material, and wherein said outer layer is formed utilizing a dielectric material.

26. The storage device in accordance with claim 24, wherein said base structure is formed utilizing a dielectric material, and wherein said outer layer is formed utilizing a conductive material.

27. The storage device in accordance with claim 24, wherein said base structure is formed utilizing a first conductive material, and wherein said outer layer is formed utilizing a second conductive material, wherein said first and said second conductive materials are different.

28. A storage device, comprising:

a p-doped semiconducting structure disposed on or in a substrate;

a substantially planar n-doped semiconducting structure disposed on said p-doped semiconducting structure forming a pn junction;

a charge trapping storage structure disposed on said n-doped semiconducting structure; and

a conductive gate, wherein said conductive gate is moveable relative to said charge trapping storage structure, wherein an electric field applied across

said n-doped semiconducting structure, said p-doped semiconducting structure and said conductive gate generates trapped charge in said charge trapping storage structure.

29. A storage device, comprising:

a pn junction disposed on or in a substrate, said junction having a buried p-doped layer and an n-doped surface layer;

a charge trapping storage layer disposed on said n-doped layer; and

a conductive gate, wherein said conductive gate and said charge trapping storage layer move relative to the other, and wherein an electric field applied across said pn junction and said conductive gate generates trapped charge in said charge trapping storage layer.

30. A storage device, comprising:

means for forming a semiconductor junction on or in a substrate, said semiconductor junction having an n-doped surface layer

means for trapping charge in a structure disposed on said n-doped surface layer; and

means for spatially localizing an electric field applied across said n-doped surface layer and said means for spatially localizing an electric field, wherein said means for spatially localizing an electric field and said structure moves relative to the other.

31. The storage device in accordance with claim 30, further comprising means for micromoving either said means for spatially localizing an electric field or said structure in at least one direction.

32. The storage device in accordance with claim 30, further comprising means for micromoving either said means for spatially localizing an electric field or said structure in two dimensions.

33. The storage device in accordance with claim 32, wherein said means for micromoving further comprises:

a frame, wherein said means for micromoving moves relative to said frame; and

suspension means for mechanically suspending said means for micromoving relative to said frame, permitting planar movement of said means for micromoving relative to said frame substantially preventing out of plane relative movement, said planar movement defined by an X-direction and a Y-direction, said suspension means including:

at least one X-axis means for flexing in response to movement of said means for micromoving in the X-direction relative to said frame, and

at least one Y-axis means for flexing in response to movement of said means for micromoving in the Y-direction relative to said frame.

34. A method of manufacturing a storage device, comprising:

creating a p-doped semiconducting layer disposed on or in a substrate;

creating an n-doped semiconducting layer disposed on said p-doped semiconducting layer;

forming a junction between said p- and n-doped semiconducting layers;

creating a charge trapping structure disposed on said n-doped semiconducting layer; and

mounting a conductive gate over said charge trapping storage layer, wherein said conductive gate and said charge trapping structure moves relative to the other, and wherein an electric field applied across said n-doped semiconducting layer and said conductive gate traps charge in said charge trapping structure.

35. The method in accordance with claim 34, wherein creating said p-doped semiconducing layer further comprises:

creating a dielectric layer on a doped substrate; and

creating an epitaxial p-doped layer on said dielectric layer.

36. The method in accordance with claim 35, wherein creating an n-doped semiconducting layer further comprises creating an epitaxial n-doped layer on said epitaxial p-doped layer.

37. The method in accordance with claim 34, wherein creating said charge trapping storage structure further comprises:

creating a first dielectric layer disposed on said n-doped semiconducting layer;

creating a second dielectric layer disposed on said first dielectric layer; and

creating a third dielectric layer disposed on said second dielectric layer.

38. The method in accordance with claim 37, wherein creating said first and said third dielectric layers further comprises creating a silicon oxide dielectric layer, and wherein creating said second dielectric layer further comprises creating a silicon nitride dielectric layer.

39. The method in accordance with claim 34, wherein creating said charge trapping storage structure further comprises creating nano-particles dispersed within a dielectric medium.

40. The method in accordance with claim 39, wherein creating nano particles further comprises creating electrically conductive nano-particles.

41. The method in accordance with claim 39, wherein creating nano particles further comprises creating germanium nano-particles dispersed within a silicon oxide layer.

42. The method in accordance with claim 34, further comprising creating a micromover coupled to either said conductive gate or said charge trapping structure, wherein said micromover moves either said conductive gate or said charge trapping structure in at least one lateral dimension.

43. The method in accordance with claim 42, wherein creating said micromover further comprises creating a micromover that moves said conductive gate relative to said charge trapping structure in at least one lateral dimension over and not in contact with said charge trapping structure.

44. The method in accordance with claim 42, wherein creating said micromover further comprises creating a micromover that moves said conductive gate relative to said charge trapping storage structure laterally in two dimensions over said charge trapping structure.

45. The method in accordance with claim 42, wherein creating said micromover further comprises:

creating a frame, wherein said micromover moves relative to said frame; and

creating a mechanical suspension having a plurality of suspension subassemblies coupled between said frame and said micromover.

46. The method in accordance with claim 45, wherein creating said mechanical suspension further comprises:

creating at lease one resilient mover flexure secured between said micromover and a coupling member; and

creating at least two resilient frame flexures secured between said coupling member and said frame, said frame flexures disposed on opposite sides of said mover flexure and aligned along a longitudinal axis passing through said mover flexure.

47. The method in accordance with claim 34, wherein mounting a conductive gate further comprises creating a conductive gate having a base structure and an outer layer formed on said base structure.

48. The method in accordance with claim 47, wherein creating said conductive gate further comprises:

forming said base utilizing a conductive material; and

forming said outer layer over said base utilizing a dielectric material.

49. The method in accordance with claim 47, wherein creating said conductive gate further comprises:

forming said base utilizing a dielectric material; and

forming said outer layer over said base utilizing a conductive material.

50. The method in accordance with claim 47, wherein creating said conductive gate further comprises:

forming said base utilizing a first conductive material; and

forming said outer layer over said base utilizing a second conductive material, wherein said first and said second conductive materials are different.

51. A method of using a storage device, comprising:

positioning a conductive gate over a charge trapping structure;

applying an electric field across an n-doped layer, said charge trapping structure, and said conductive gate proximate to said charge trapping storage structure, said charge trapping layer disposed on said n-doped layer and said n-doped layer disposed over a substrate; and

generating a localized trapped charge region in said charge trapping structure.

52. The method in accordance with claim 51, wherein applying said electric field further comprises applying an electric field across a p-doped layer disposed between said n-doped layer and said substrate.

53. The method in accordance with claim 52, wherein applying an electric field across said p-doped layer further comprises applying a positive voltage to said conductive gate, a negative voltage to said p-doped layer and about zero volts to said n-doped layer.

54. The method in accordance with claim 52, wherein applying an electric field across said p-doped layer further comprises applying an electric field across said p-doped layer and said n-doped layer to operate at or near an avalanche breakdown region.

55. The method in accordance with claim 51, wherein positioning said conductive gate further comprises moving either said conductive gate or said charge trapping structure so that said conductive gate is over a predetermined data storage location on said charge trapping structure.

56. The method in accordance with claim 55, wherein moving either said conductive gate or said charge trapping structure further comprises moving either said conductive gate or said charge trapping structure in at least one lateral direction while applying said electric field across said n-doped layer and said charge trapping structure.

57. The method in accordance with claim 55, wherein moving either said conductive gate or said charge trapping structure further comprises moving either said gate or said charge trapping structure in two-dimensions.

58. The method in accordance with claim 51, further comprising measuring the amount of charge in said localized trapped charge region.

59. The method in accordance with claim 58, further comprising moving either said conductive gate or said charge trapping structure in at least one dimension while measuring the amount of charge.

60. The method in accordance with claim 58, wherein measuring the amount of charge further comprises determining the capacitance between said conductive gate and said charge trapping structure.

61. The method in accordance with claim 51, further comprising removing said localized trapped charge region.

62. The method in accordance with claim 61, further comprising forward biasing said p-doped layer and said n-doped layer whereby said localized trapped charge region is removed.